L Number	Hits	Search Text	DB	Time stamp
37	27425	chalcogenide or GeSbTe or (phase adj change)	USPAT; US-PGPUB	2003/04/29 16:13
38	10	(chalcogenide or GeSbTe or (phase adj change)) and HSG	USPAT; US-PGPUB	2003/04/29 16:13
39	11844	chalcogenide or GeSbTe or (phase adj change)	EPO; JPO; DERWENT; IBM_TDB	2003/04/29 16:13
40	0	(chalcogenide or GeSbTe or (phase adj change)) and HSG	EPO; JPO; DERWENT; IBM_TDB	2003/04/29 16:13

US-PAT-NO: 6461967

DOCUMENT-IDENTIFIER: US 6461967 B2

TITLE: Material removal method for forming a structure

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As an example of one such shaped structure which is in need of being formed with reduced size is an ovonic cell of a programmable resistor. An ovonic cell is a region of **chalcogenide** material that has a resistance which is programmable by an electrical charge passed through the ovonic cell. Generally, the ovonic cell is formed by etching out an opening from a volume of material, and thereafter depositing the **chalcogenide** material into the opening. As a high charge density is most suitable for programming the ovonic cell, it is desirable that the opening be formed with a small cross-sectional area, which serves to increase the density of a charge applied thereto. The opening is conventionally patterned with photolithography. It would be desirable to find a commercially feasible method of forming the opening with a width narrower than about 0.2 microns.

As a result of the etching process which is selective to implanted silicon-containing material, a selected portion of the polysilicon layer that is not implanted up to the threshold concentration of ions is etched away to form a shaped opening. Etching process parameters, such as the duration of the etch, can also be varied to further tailor the shaped opening. In one example of the use of a shaped opening, an ovonic cell of a programmable resistor is formed by filling the shaped opening with **chalcogenide** material.

FIG. 9 is a cross-sectional view of the semiconductor wafer of FIG. 8,

showing **chalcogenide** material of a programmable resistor formed in the shaped opening of FIG. 8.

FIG. 68 is a cross-sectional view of the semiconductor wafer of FIG. 66, showing a further procedure of the fourteenth method of the present invention in which an etching process is conducted which is selective to implanted silicon-containing material to remove the unimplanted inner portion of the polysilicon layer and in which **HSG** polysilicon is deposited on the inner and outer faces of a free-standing wall formed thereby.

One application of the use of the embodiment of FIGS. 7 through 9 of forming shaped openings to form a hard mask is shown in FIG. 9, wherein polysilicon layer 14 has been removed, and the further procedures of depositing and patterning a material in hole 36 has been conducted. The material deposited in hole 36 in this embodiment comprises ovonic **chalcogenide** material, and forms a plug 38 suitable for use in a programmable resistor. This embodiment thus meets the need for forming **chalcogenide** programmable resistors in a hole having sub-photolithography resolution dimensions.

In a further alternative embodiment also shown in FIG. 19, shaped polysilicon structure 54 is removed to form a shaped opening. In forming the shaped opening, shaped polysilicon structure 54 is removed with an etching process that etches polysilicon selective to silicon dioxide layer 62. The resulting shaped opening, illustrated in the form of a hole 64, is suitable for making contact between underlying silicon substrate 42 and the surface of silicon dioxide layer 62. Hole 64 could also be filled with **chalcogenide** material, as in the embodiment of FIG. 9 in the first method, to form an ovonic cell of a programmable resistor.

As illustrated in FIG. 42, conventional process flow is initially followed under the ninth method until gate regions are formed. As shown, a semiconductor substrate is provided in the form of a semiconductor wafer 180. Semiconductor wafer 180 is formed with a silicon substrate 190 thereon, upon which is formed active regions 180a adjoined by gate regions 182. A dielectric

layer such as a TEOS layer 182a is formed over active regions 180a and gate regions 182. A polysilicon layer 184 is deposited over TEOS layer 182a. Polysilicon layer 184 is formed of intrinsic polysilicon as described above, and could comprise **HSG** polysilicon. Above polysilicon layer 184 is formed a hard mask layer, such as a silicon nitride hard mask layer 186. The hard mask layer serves as both a hard mask for an ion implantation process and as an etch barrier for a subsequently conducted height reduction process. Silicon dioxide is also a suitable material for forming the hard mask layer.

Once the ion implantation operation is conducted, the etching process is conducted which is selective to implanted silicon-containing material of the present invention. The etching process is conducted substantially in the same manner as described above for the first method. Consequently, the unimplanted polysilicon of first polysilicon layer 184 is removed, leaving conical structures 194 seen in FIG. 45. Conical structures 194 are free-standing and preferably have an aspect ratio greater than about 2 to 1. As such, conical structures 194 can be designed to have a relatively small surface area contact to active region 180a, and are suitable for use as stacked capacitor storage nodes. **HSG** or CSG polysilicon may also be deposited on the surface of conical structures 194 so as to increase the surface area thereof.

The surface of the stacked capacitor storage node is, under the fourteenth method, roughened in order to increase the surface area thereof. The inner surface of the stacked capacitor storage node can be roughened after removal of photoresist plug 328, while either of both the inner and outer surfaces of polysilicon layer 320 can be roughened after formation of open space 330. Roughening the surface of polysilicon layer 320 results in a greater surface area per square centimeter than a non-roughened surface, thereby increasing charge retention of the completed capacitor. The roughened surface is preferably obtained by depositing a layer of hemispherical grain (**HSG**) polysilicon or cylindrical grain polysilicon (CSG) on the surface of polysilicon layer 320. The **HSG** polysilicon or CSG polysilicon layer is preferably deposited selectively with CVD in a manner known in the art. Summarily, this comprises depositing a thin undoped or lightly doped layer of

amorphous silicon over polysilicon layer 20 and subsequently applying a high pressure and temperature. The high pressure and temperature result in a nucleation of the amorphous silicon layer into discrete grains.

L Number	Hits	Search Text	DB	Time stamp
2	999	(chalcogenide or GeSbTe or (phase adj change)) and (interfacial or adhesion) and (dielectric or insulating or insulative or insulator)	USPAT; US-PGPUB	2003/04/29 11:28
3	908	((chalcogenide or GeSbTe or (phase adj change)) and (interfacial or adhesion) and (dielectric or insulating or insulative or insulator)) and @ad<=20011231	USPAT; US-PGPUB	2003/04/29 11:42
4	478	(((chalcogenide or GeSbTe or (phase adj change)) and (interfacial or adhesion) and (dielectric or insulating or insulative or insulator)) and @ad<=20011231) and (polysilicon or silicon or HSG)	USPAT; US-PGPUB	2003/04/29 11:42
5	18	(chalcogenide or GeSbTe or (phase adj change)) and (interfacial or adhesion) and (dielectric or insulating or insulative or insulator)	EPO; JPO; DERWENT; IBM_TDB	2003/04/29 11:58
8	1393	438/93-95,398,602.ccls.	USPAT; US-PGPUB	2003/04/29 11:53
9	1263	438/93-95,398,602.ccls. and @ad<=20011231	USPAT; US-PGPUB	2003/04/29 11:42
10	1010	(438/93-95,398,602.ccls. and @ad<=20011231) and (polysilicon or silicon or HSG)	USPAT; US-PGPUB	2003/04/29 11:43
11	44	((438/93-95,398,602.ccls. and @ad<=20011231) and (polysilicon or silicon or HSG)) and (chalcogenide or GeSbTe or (phase adj change))	USPAT; US-PGPUB	2003/04/29 12:00
16	87	257/3,4,200,246.ccls. and (chalcogenide or GeSbTe)	USPAT; US-PGPUB	2003/04/29 12:06

DERWENT-ACC-NO: 2001-126796

DERWENT-WEEK: 200114

TITLE: **Phase change** type magneto-optical disk has transparent layer made of silicon, carbon, oxygen, nitrogen, where sum of atom percentage of each element is equal to cent percent

PATENT-ASSIGNEE: KYOCERA CORP[KYOC]

PRIORITY-DATA: 1999JP-0022113 (January 29, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000222789 A	August 11, 2000	N/A	006	G11B 011/10

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2000222789A	N/A	1999JP-0022113	January 29, 1999

INT-CL (IPC): G11B007/24, G11B011/10

ABSTRACTED-PUB-NO: JP2000222789A

BASIC-ABSTRACT:

NOVELTY - The transparent **dielectric** layer (2) formed on resin substrate (1) is made of Si_a, C_b, O_c and N_d, where a=37-47 atom%, b=3-9 atom%, c=6-18 atom%, d=26-54 atom% such that overall atom% that is a+b+c=100 atom%.

DETAILED DESCRIPTION - A transparent **dielectric** layer (2), a magneto-optical recording layer (3), another transparent **dielectric** layer (4) and reflex layer (5) are laid sequentially on transparent resin substrate (1).

USE **- Phase change** type magneto-optical disk.

ADVANTAGE - Since **adhesion** of transparent **dielectric** layer on transparent resin substrate is high, carrier-to-noise ratio and Kerr-rotation angle are improved.

DESCRIPTION OF DRAWING(S) - The figure shows the fragmentary sectional view of magneto-optical disk.

resin substrate 1

transparent **dielectric** layers 2,4

magneto-optical recording layer 3

reflex layer 5

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: **PHASE CHANGE** TYPE MAGNETO OPTICAL DISC TRANSPARENT LAYER MADE SILICON CARBON OXYGEN NITROGEN SUM ATOM PERCENTAGE ELEMENT EQUAL CENT

DERWENT-CLASS: L03 T03 W04

CPI-CODES: L03-B05F; L03-G04B;

EPI-CODES: T03-D01A1A; T03-D01A3E; W04-D01A;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2001-037050
Non-CPI Secondary Accession Numbers: N2001-093542

DERWENT-ACC-NO: 1999-105863

DERWENT-WEEK: 200037

TITLE: Diamond like carbon outer coating for optical recording media - is ion beam deposited in a vacuum deposition chamber onto a composite optical **phase change** recording layer

INVENTOR: BROWN, D W; MAHONEY, L J ; PETRMICHL, R H ; THEAR, E G

PATENT-ASSIGNEE: DIAMONEX INC[MONS] , MONSANTO CO[MONS]

PRIORITY-DATA: 1997US-0886922 (July 2, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 9901277 A1	January 14, 1999	E	020	B32B 003/00
US 6086796 A	July 11, 2000	N/A	000	B29D 017/00

DESIGNATED-STATES: CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
WO 9901277A1	N/A	1998WO-US06506	March 31, 1998

US 6086796A N/A 1997US-0886922 July 2, 1997

INT-CL (IPC): B29D017/00, B32B003/00 , B32B003/02

ABSTRACTED-PUB-NO: US 6086796A

BASIC-ABSTRACT:

A method (I) for producing protective coatings on a recording media surface for near-field optical head devices comprises: (a) depositing a composite optical **phase-change** recording layer onto a structure; (b) ion beam depositing a diamond like carbon (DLC) outer layer of 450 Angstroms maximum thickness on the recording layer in an evacuated deposition vacuum chamber; and (c) increasing the chamber pressure to atmosphere pressure.

Also claimed is a method similar to (I) further comprising depositing firstly a **dielectric** interlayer onto the recording layer and secondly an **adhesion**-promoting interlayer onto the **dielectric** in a vacuum chamber prior to the deposition of the DLC layer where the combined maximum thickness of DLC layer, and both interlayers is 500 Angstroms.

USE - Used for optical recording media, particularly those having a near-field optical head device used in optical read/write apparatus.

ADVANTAGE - The protective outer layer is highly adherent with greatly improved resistance to wear, abrasion, corrosion and environmental durability. The method allows mass deposition at low cost of such coatings. The coating has improved lifetime, high density and extreme surface smoothness and has high reproducibility of thickness and uniformity.

ABSTRACTED-PUB-NO: WO 9901277A

EQUIVALENT-ABSTRACTS:

A method (I) for producing protective coatings on a recording media surface for near-field optical head devices comprises: (a) depositing a composite optical **phase-change** recording layer onto a structure; (b) ion beam depositing a diamond like carbon (DLC) outer layer of 450 Angstroms maximum thickness on the recording layer in an evacuated deposition vacuum chamber; and (c) increasing the chamber pressure to atmosphere pressure.

Also claimed is a method similar to (I) further comprising depositing firstly a **dielectric** interlayer onto the recording layer and secondly an **adhesion**-promoting interlayer onto the **dielectric** in a vacuum chamber prior to the deposition of the DLC layer where the combined maximum thickness of DLC layer, and both interlayers is 500 Angstroms.

USE - Used for optical recording media, particularly those having a near-field optical head device used in optical read/write apparatus.

ADVANTAGE - The protective outer layer is highly adherent with greatly improved resistance to wear, abrasion, corrosion and environmental durability. The method allows mass deposition at low cost of such coatings. The coating has improved lifetime, high density and extreme surface smoothness and has high reproducibility of thickness and uniformity.

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS: DIAMOND CARBON OUTER COATING OPTICAL RECORD MEDIUM ION BEAM DEPOSIT VACUUM DEPOSIT CHAMBER COMPOSITE OPTICAL **PHASE CHANGE** RECORD LAYER

DERWENT-CLASS: L03 P73

CPI-CODES: L03-G04B; L03-J;

UNLINKED-DERWENT-REGISTRY-NUMBERS: 1669U; 1776U

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1999-031627
Non-CPI Secondary Accession Numbers: N1999-076382

US-PAT-NO: 6512241

DOCUMENT-IDENTIFIER: US 6512241 B1

TITLE: **Phase change** material memory device

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A **phase change** memory with a very limited area of contact between the lower electrode and the **phase change** material may be formed by defining a closed geometric structure for the lower electrode. The lower electrode may then be covered. The covering may then be opened in a very narrow strip extending across the closed geometric shape using phase shift masking. A **phase change** material may be formed in the opening. Because the opening effectively bisects the closed geometric structure of the lower electrode, two very small contact areas may be created for contacting the lower electrode to the **phase change** material.

Phase change material memory device

This invention relates generally to electronic memories and particularly to electronic memories that use **phase change** material.

Phase change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure. Generally any **phase change** material may be

utilized. In some embodiments, however, thin-film chalcogenide alloy materials may be particularly suitable.

The **phase change** may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter, or vice versa, in response to temperature changes. In effect, each memory cell may be thought of as a programmable resistor, which reversibly changes between higher and lower resistance states. The **phase change** may be induced by resistive heating.

A variety of **phase change** alloys are known. Generally, chalcogenide alloys contain one or more elements from Column VI of the periodic table. One particularly suitable group of alloys is the GeSbTe alloys.

A **phase change** material may be formed within a passage or pore through an insulator. The **phase change** material may be coupled to upper and lower electrodes on either end of the pore.

Ideally, the area of contact between the lower electrode and **phase change** material should be made as small as possible. This is because the resistance is a function of the contact area. Generally, the smaller the contact area, the higher the resistance. Higher resistance means more effective heating for this same electrical current. Ideally, the minimum amount of electrical current is supplied to each device to make the memory as power conserving as possible.

Thus, there is a need for better ways to reduce the effective size of the lower electrode in **phase change** memories.

Referring to FIG. 1, a **phase change** memory cell 10 may be formed on the substrate 12 that, in one embodiment, may be a silicon substrate. A buried conductive layer 13 may be formed in a substrate 12. In one embodiment, the buried conductive layer 13 may act as a row or column of a memory array.

A **phase change** material 20 may contact the upper edges of the sides 16a of the lower electrode 16. An upper electrode 22 may be defined over the **phase change** material 20. A portion of the upper electrode 22 and the **phase change** material 20 may rest over a glue layer including a conductive material 28 and an insulator 26. The conductive material 28 may be polysilicon and the insulator 26 may be an oxide in one embodiment of the present invention.

Thus, referring to FIG. 2, the upper electrode 22 may be defined over a region covered by the conductive layer 28 that may act as part of a glue layer to adhere the **phase change** material 20. The lower electrode 22 and the **phase change** material 20 extend from an upper plateau defined by the glue layer, downwardly through an opening 30 in the glue layer to make direct electrical contact with the lower electrode 16. In this case, the lower electrode 16 may be can-shaped, defining a closed geometrical edge, only a small portion of which makes electrical contact with the **phase change** material 20.

As shown in FIG. 6, an insulator layer 26, such as an oxide layer, may be defined over the resulting structure shown in FIG. 5. Thereafter, a glue layer 28 may be formed to improve the **adhesion** between a **phase change** material (yet to be formed) and the rest of the structure. In one embodiment, the layer 28

may be polysilicon.

As a result, only a very small region 16c (which may be square) of the electrode 16 is exposed through the opening 30. One of the exposed regions 16c forms a very small electrical contact to the **phase change** material as will be explained next.

Referring to FIG. 9, a **phase change** material 20, such as a chalcogenide, may be formed over the resulting structure. Next, a conductive material may be formed over the entire structure to eventually form the upper electrode 22. Then, the **phase change** material 20 and the upper electrode 22 may be masked and etched to form the structure shown in FIGS. 1 and 2.

It may be appreciated that a very small contact 16c may be defined in this way. In fact, the size of the region 16c may be smaller than the minimum feature size available with lithographic techniques. This may greatly increase the resistance of the resulting contact and may improve the performance of the **phase change** memory in some embodiments.

1. A **phase change** memory comprising: an electrode on said substrate, said electrode having a substantially planer surface with a closed geometric shape; a layer covering substantially all of the closed geometric shape with the exception of an exposed portion; and a **phase change** material contacting said exposed portion.

8. The memory of claim 1 wherein said layer includes an **adhesion** promoting layer.

10. The memory of claim 9 including an opening through said **adhesion** promoting layer and said insulator to form said exposed

portion.

11. A memory comprising: an electrode having a length; a layer over said
electrode; an opening through said layer to expose only a portion of said
electrode, said opening extending across the length of said electrode generally
transverse to the length of said electrode; and a **phase change** material over
said layer and extending through said opening to contact said electrode.

15. The memory of claim 11 wherein said layer includes an **adhesion**
promoting material.

16. The memory of claim 15 wherein said layer includes an insulating
material under said **adhesion** promoting material.

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☒	US 20030047762 A1	20030313	7	Phase change material memory device	257/276
2	☐	☒	US 20030047727 A1	20030313	9	USING SELECTIVE DEPOSITION TO FORM PHASE-CHANGE MEMORY CELLS	257/3
3	☐	☒	US 20030041452 A1	20030306	16	Filling plugs through chemical mechanical polish	29/852
4	☐	☒	US 20030015722 A1	20030123	36	Structure and method for fabricating semiconductor structures and devices for dispersing a radiant energy transmission	257/103
5	☐	☒	US 20030001242 A1	20030102	30	Adhesive material for programmable device	257/646
6	☐	☒	US 20020181915 A1	20021205	37	Apparatus for generating an oscillating reference signal and method of manufacture therefore	385/131
7	☐	☒	US 20020179936 A1	20021205	22	Structure and method for fabricating semiconductor structures and devices which include quaternary chalcogenides	257/200
8	☐	☒	US 20020080647 A1	20020627	23	Metal structure for a phase-change memory device	365/175
9	☐	☒	US 20020045323 A1	20020418	64	Method for making programmable resistance memory element	438/382
10	☐	☒	US 20020039306 A1	20020404	25	Single level metal memory cell using chalcogenide cladding	365/100

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	257/751; 257/758; 257/763; 257/773		Lowrey, Tyler A.	☒	☐	☐	☐	☐	☐	☐	US 20030047762	☐
2	257/2; 257/4; 438/900		Chiang, Chien	☒	☐	☐	☐	☐	☐	☐	US 20030047727	☐
3	29/831; 29/846		Sinha, Nishant	☒	☐	☐	☐	☐	☐	☐	US 20030041452	☐
4			Chason, Marc et al.	☒	☐	☐	☐	☐	☐	☐	US 20030015722	☐
5			Lowrey, Tyler A. et al.	☒	☐	☐	☐	☐	☐	☐	US 20030001242	☐
6	385/14		Craig, Ronald A. et al.	☒	☐	☐	☐	☐	☐	☐	US 20020181915	☐
7			Droopad, Ravindranath	☒	☐	☐	☐	☐	☐	☐	US 20020179936	☐
8			Chiang, Chien et al.	☒	☐	☐	☐	☐	☐	☐	US 20020080647	☐
9			Lowrey, Tyler et al.	☒	☐	☐	☐	☐	☐	☐	US 20020045323	☐
10			Lowrey, Tyler A.	☒	☐	☐	☐	☐	☐	☐	US 20020039306	☐

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
11	☐	☒	US 20020036931 A1	20020328	40	Electrically programmable memory element with reduced area of contact and method for making same	365/200
12	☐	☒	US 20010049074 A1	20011206	23	Optical information recording medium and optical recording method	430/270.13
13	☐	☒	US 6545287 B2	20030408	8	Using selective deposition to form phase-change memory cells	257/3
14	☐	☒	US 6512241 B1	20030128	6	Phase change material memory device	257/4
15	☐	☒	US 6500733 B1	20021231	24	Synthesis of layers, coatings or films using precursor layer exerted pressure containment	438/459
16	☐	☒	US 6495067 B1	20021217	28	Liquid crystal compound, liquid crystal mixture or composition, electrolyte comprising the same, electrochemical cell and photo-electrochemical cell containing the electrolyte	252/299.61
17	☐	☒	US 6445675 B1	20020903	15	Phase change optical recording medium and process for manufacturing same	369/275.2
18	☐	☒	US 6404665 B1	20020611	25	Compositionally modified resistive electrode	365/100

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
11			Lowrey, Tyler et al.	☒	☐	☐	☐	☐	☐	☐	US 20020036931	☐
12	369/275.2; 369/275.5; 428/64.6; 430/945		Ohno, Takashi et al.	☒	☐	☐	☐	☐	☐	☐	US 20010049074	☐
13	257/2; 257/289; 438/900		Chiang, Chien	☒	☐	☐	☐	☐	☐	☐	US 6545287	☐
14	257/3		Lai, Stefan K.	☒	☐	☐	☐	☐	☐	☐	US 6512241	☐
15	156/289; 419/45; 438/455; 438/763		Stanbery, Billy J.	☒	☐	☐	☐	☐	☐	☐	US 6500733	☐
16	136/263; 252/299.2; 252/299.3; 252/62.2; 429/328; 546/347; 548/335.1		Ono, Michio	☒	☐	☐	☐	☐	☐	☐	US 6495067	☐
17	369/288; 428/64.1; 430/273.1		Ebina, Atsushi et al.	☒	☐	☐	☐	☐	☐	☐	US 6445675	☐
18	257/3; 257/4; 257/5; 257/E29.17; 365/148; 365/163		Lowrey, Tyler A. et al.	☒	☐	☐	☐	☐	☐	☐	US 6404665	☐

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
19	☐	☒	US 6350946 B1	20020226	29	Photoelectric conversion device and photoelectric cell	136/252
20	☐	☒	US 6312779 B1	20011106	27	Information recording medium and information recording/reproducing apparatus	428/64.1
21	☐	☒	US 6141315 A	20001031	13	Phase change optical recording medium containing oxygen and process for manufacturing the same	369/275.2

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
19	136/256; 136/258; 136/263; 257/43; 257/431; 257/49; 423/598; 423/608; 423/610; 423/622; 427/74; 429/111; 438/82; 438/85		Miyake, Kiyoteru et al.	☒	☐	☐	☐	☐	☐	☐	US 6350946	☐
20	369/283; 369/288; 428/64.4; 428/64.5; 428/64.6; 428/913; 430/270.13; 430/495.1; 430/945		Hirotsune, Akemi et al.	☒	☐	☐	☐	☐	☐	☐	US 6312779	☐
21	430/273.1		Ebina, Atsushi et al.	☒	☐	☐	☐	☐	☐	☐	US 6141315	☐

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☒	EP 1178477 A	20020206	20	Phase change optical recording medium has recording layer with material containing oxygen content of specific atomic percentage with respect to recording layer	
2	☐	☒	JP 2000222789 A	20000811	6	Phase change type magneto-optical disk has transparent layer made of silicon, carbon, oxygen, nitrogen, where sum of atom percentage of each element is equal to cent percent	
3	☐	☒	US 6086796 A	19990114	13	Diamond like carbon outer coating for optical recording media - is ion beam deposited in a vacuum deposition chamber onto a composite optical phase change recording layer	
4	☐	☒	EP 874361 A	20020903	13	Phase change optical recording medium - comprises substrate, transparent dielectric layer, recording layer comprising material containing oxygen and further transparent dielectric layer	
5	☐	☒	EP 779614 A	19970618	9	Phase change optical recording medium - uses light irradiation to change the phase of the recording layer during reading, writing, or erasure	

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1			EBINA, A et al.	☒	☐	☐	☐	☐	☐	☐	EP 1178477 A1	☐
2				☒	☐	☐	☐	☐	☐	☐	JP 2000222789 A	☐
3			BROWN, D W et al.	☒	☐	☐	☐	☐	☐	☐	US 6086796	☐
4			EBINA, A et al.	☒	☐	☐	☐	☐	☐	☐	US 6141315	☐
5			ADACHI, K et al.	☒	☐	☐	☐	☐	☐	☐	US 5912103	☐